- - Figure 2 illustrates RF front end 107, which includes monolithic and discrete elements. The electronics of the GPS receiver 106 are typically implemented as a fully custom Radio Frequency Integrated Circuit [[.]] (RFIC), coupled to a GPS processor or GPS engine implemented using digital ASIC technology. One such GPS engine is described in U.S. Patent No. 5,897,605, which is incorporated by reference herein. The GPS signals 104A-104C are typically received by a GPS antenna 200, and are then applied to an LNA or section 202. The LNA 202 may be fully included in the RFIC or may be distributed between the RFIC and an external amplifier, to achieve a better noise figure. The LNA section 202 may have an input filter to limit unwanted signals which may cause receiver interference. The LNA 202 may use an output filter 204 to limit the unwanted out of band signals. U.S. Patent No. 4,701,934, issued to Jasper, which is incorporated by reference herein, presents a system where the LNA output filter 204 is used as the receiver noise bandwidth setting filter, but in the implementation described in the Jasper patent, this filter 204 is also used to attenuate out of band intermodulation products and high level out of band spurious signals that could cause receiver 106 performance degradation. - -

Please replace the paragraph beginning on page 8, line 12 and ending on page 9, line 5, which begins with the phrase "In the present invention the noise bandwidth of the receiver 106" with the following rewritten paragraph:

- - In the present invention the noise bandwidth of the receiver 106 is set in an [[the]] IF filter 206 following an [[the]] image reject mixer 208. In the preferred embodiment, the 6 dB bandwidth of the IF filter 206 is nominally 6 MHz. The output from an [[the]] internal LNA 210

is applied to the input of the [[an]] image reject mixer 208. The image reject mixer 208 comprises 2 double-balanced mixers 212 and 214 with In-phase LO (I-LO) and Quadrature-phase LO (Q-LO) inputs, and I-IF and Q-IF outputs, I and Q Active Filter Circuits 206 and a combiner circuit (phase shift network) 216. The I-IF and Q-IF outputs are combined using phase shift network 216 to obtain a single IF output. The L1 GPS signal, which is centered at 1575.42 MHz, is down-converted to the IF frequency at approximately 9.5 MHz by the [[an]] image reject mixer 208. An [[The]] IF AGC amplifier 218 boosts the IF signal to the proper level for quantizing by a 2 bit A/D converter 222. The IF AGC amplifier 218 gain is controlled from the digital processing section in the digital ASIC 110 (FIG. 1), by way of an AGC control block 220. The sample clock for the A/D converter 222 is provided by an [[the]] ACQCLK signal 252, which is generated by a [[the]] Divide by 41 section 224 which is synthesized by a Phase Locked Loop (PLL) locked to a [[the]] crystal oscillator 226, which provides a reference signal. Typically, the ACQCLK signal 252 has a frequency approximately equal to 37.3333fo, where fo = 1.023 MHz. In the preferred embodiment, the digitized GPS information bearing signal is provided as 2-bit Positive ECL (PECL) levels by PECL buffers 254, 256 and sent to the digital ASIC 110. - -

Please replace the paragraph on page 9, lines 6-18, which begins with the phrase "The synthesizer section 227" with the following rewritten paragraph:

- - A [[The]] synthesizer section 227 of the RF front end 107 is typically entirely contained in the RFIC except for [[the]] loop filter components 228, and the support components of [[the]] crystal oscillator active circuitry 230. The crystal oscillator section can be

implemented using a crystal resonator 226, or using a signal from an external Temperature Compensated crystal Oscillator (TCXO). The crystal resonator 226 frequency is typically nominally 24.5535 MHz, and can vary by 40 parts per million (ppm) around this frequency. The reference oscillator 230 frequency is doubled by a frequency doubler 232 and then divided by 9 by a divider 234. Of course, the crystal oscillator 230 can generate a frequency of twice that of 24.5535 MHz, which eliminates the need for the frequency doubler 232. The doubled frequency (or direct frequency if it is already generated) is also sent to a PECL output buffer 260 to provide a signal 236, typically named GPSCLK, which is a GPS clock signal used by the digital ASIC 110. Typically, the GPSCLK signal 236 has a frequency of approximately 48fo, where fo = 1.023 MHz. The divided-by-9 signal is applied to a phase/frequency detector 238 for the reference input of the phase-lock-loop. - -

Please replace the paragraph beginning on page 9, line 19, and ending on page 10, line 4, which begins with the phrase "A voltage controlled oscillator" with the following rewritten paragraph:

- - A voltage controlled oscillator (VCO) 242 that operates at a typical nominal frequency of 1565.97 MHz is implemented entirely within the RFIC, and provides 3 output signals. A monolithic VCO, such as described in U.S. Patent No. 5,917,383, which is incorporated by reference herein, may be used. The I and Q outputs of this oscillator 242 are sent to the mixers 212 and 214, and the P output 244 to the [[a]] divider 224. This divider 224 takes the output signal 244 of the VCO 242 [[244]] and divides it by 41. The output of this divider 224 is used as the 2-bit A/D sample clock, and is also provided as an RFIC output, ACQCLK signal 252. The divider 224 output is also further divided by 7 at divider 246, and the [[with]] output of divider 246 is sent to the phase/frequency detector 238 as the feedback signal for the phase-locked loop (PLL) synthesizer. - -

Please replace the paragraph on page 10, lines 5-8, which begins with the phrase "The output of the phase/frequency detector" with the following rewritten paragraph:

- - The output of the phase/frequency detector 238 is applied to a charge pump section 240. The charge pump section 240 is internal to the RFIC, with the loop filter 228 implemented externally to the RFIC, with passive components. The output of the loop filter 228 is used to control the frequency and phase of signals provided by VCO 242. - -

Please replace the paragraph on page 10, lines 9-14, which begins with the phrase "The sampled SIGN and MAG digital signals 248 and 250" with the following rewritten paragraph:

- - Sampled ~~The sampled~~ SIGN and MAG digital signals 248 and 250, respectively, are provided to PECL buffers 254 and 256 to send the signal to the GPS digital ASIC 110 for digital processing. The near one-quarter ratio of the IF frequency and the ACQCLK signal 252 allow for generation of "near baseband" I and Q signals representing the GPS signal using the sampling and decimation method described in the aforementioned 5,897,605 patent. Interface buffers 254-260 are used to provide PECL signals to the GPS digital ASIC 110. - -

Please replace the paragraph on page 10, lines 15-19, which begins with the phrase "The system of the present invention is differentiated from the system" with the following rewritten paragraph:

- - The system of the present invention is differentiated from the system described in the Jasper patent in the generation and control of the LO, the IF filtering, the image reject mixing, and the A/D conversion process, and that the RFIC of the present invention is designed to implemented with a very [[a]] high level of integration. This is accomplished by setting the noise bandwidth of the receiver 106 using the IF filter 206 following the dual mixers 208. - -

Please replace the paragraph beginning on page 10, line 21, and ending on page 11, line 8, which begins with the phrase "In FIG. 3, bias control 300" with the following rewritten paragraph:

- - In FIG. 3, bias control 300 is used to power down portions of RFIC 108 depending on which circuits within the RFIC 108 are needed to receive and/or process signals as determined from the digital ASIC 110, or some other portion of receiver 106. For example, since the implementations ~~implementation~~ of RF front end 108 shown in FIGS. 2 and 3 use an IF filter section, which comprises mixer 208, Filter 206, and combiner 216, typically use an IF frequency centered at about 9.5 MHz, such an approach allows some of these sections, namely everything shown in FIG. 3 except the crystal oscillator 230, the X2 frequency doubler 232, and the GPSCLK PECL drivers 260 and reference 262 to the turned off when not needed, e.g., when the GPS signals 104A-104C (FIG. 1) are not being received, but a processing clock is still required for processing the signals on the digital ASIC 110. This approach minimizes the power consumption of the portion of receiver 106 shown in FIG. 3, depending on the state of the RF front end 107. - -

Please replace the paragraph on page 11, lines 13-22, which begins with the phrase "As described herein, the present invention allows for a PECL interface" with the following rewritten paragraph:

- - As described herein, the present invention allows for a PECL interface between the RF front end 108 IC and the digital ASIC (processing section) 110 for some signals. Such an interface comprises an acquisition clock (ACQ CLK or CLK ACQ) signal 400, a GPS Clock (GPS CLK or CLK GPS) signal 402, a SIGN signal 404, a MAG signal 406, and a reference (PECL REF or REF) signal 408. The interface also comprises non-PECL signals from the digital ASIC 110 to the RFIC 108, such as an [[a]] AGC Data (AGC DATA or AGCDAT) signal 410. The interface may also comprise a power management (PWR MGMT) signal 412 that is usually input into the bias control 300. Signal 412 is typically used to turn the RF front end 108 on and off based on the needs of the receiver or system. The power management signal 412 is typically a low bandwidth, low-power signal, such as a CMOS control signal. - -